Datasheet

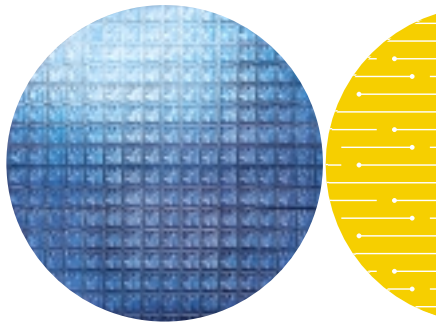
Intel® Dialogic® SingleSpan-JCT Series

Intel® Dialogic® SingleSpan-JCT boards provide one span of digital network interfaces in a H.100-compliant universal PCI form factor. The boards contain rich media features such as voice processing, speech recognition software, fax, tone signaling, global tone detection, global tone generation, and call progress analysis, making them ideal for service providers and large enterprises.

Features and Benefits

- High channel-per-slot density: one T-1 ISDN PRI trunk with 24 channels of voice processing or one E-1 ISDN PRI trunk with 30 channels of voice processing
- Supports continuous speech processing[1]: a flexible speech processing technology, coupled with efficient drivers, off-loads critical real-time signal processing in speech-enabled applications to onboard DSPs. Reduces system latency, increases recognition accuracy, and improves overall system response time for high-density speech solutions.
- Supports DSP-based onboard fax and host-based speech recognition to maximize the number of boards in the system[2]
- Supports G.726 bit exact and GSM coders, letting developers implement unified messaging applications that meet VPIM standards
- Offered in industry-standard 32-bit PCI form factor with universal connector
- Silence-compressed recording eliminates silence and preserves hard disk space
- H.100 connector lets developers take advantage of the industry-standard CT Bus and increases the board's capacity to interoperate with other CT Bus-compatible boards
- Downloadable signal and call processing firmware provides easy feature enhancement and field-proven performance based on over four million installed ports
- Unified call control access through Global Call interface provides worldwide application portability and shortens development time by using the same API for almost any network protocol
- Intel® Dialogic® CT Media™ server software support facilitates multiapplication development
- Supports the Board Watch tool, the SNMP-compatible software for remote CT board management
- Enables system integrators and developers to lower costs by incorporating more ports per chassis, using less expensive desktop-style machines, and easing configuration/installation effort
- Software development kits (SDKs) for Windows NT*, Windows* 2000, and Linux* yield faster time to market

[1]Please refer to the continuous speech processing datasheet for more information.
[2]Fax and host-based speech recognition are mutually exclusive.



Intel in Communications

The Intel® Dialogic® D/240JCT-T1, D/300JCT-E1, D/480JCT-1T1, and D/600JCT-1E1 boards are the next generation of SingleSpan products based on Spring Ware firmware. They are ideal for developers seeking to provide cost-effective, highly scalable, high-density communications applications requiring multimedia resources such as voice, software-based speech recognition, fax, and digital network interface in a single personal computer (PC) slot. These boards offer a rich set of advanced features and support digital signal processing (DSP) technology and industry-standard PCI bus and CT Bus technologies.

Support for the innovative continuous speech processing technology enables seamless integration of software-based speech recognition software from leading speech technology vendors. Onboard DSP-based fax and support for software-based speech recognition lets developers maximize the number of boards in the system for multimedia communications applications such as Web-enabled call centers, voice portals, unified messaging, or speech-enabled interactive voice response (IVR). The option to use new voice coders such as GSM and G.726 (the de facto standards when complying with Voice Profile for Internet Messaging [VPIM] standards) provides the capability to build unified messaging solutions while working with existing legacy messaging systems. In addition, support under Global Call and Intel® Dialogic® CT Media™ software facilitates global deployment and adds the flexibility to scale systems to meet the growing needs of your business.

Configurations

Use Intel Dialogic SingleSpan-JCT boards to develop sophisticated, multimedia communications systems incorporating capabilities such as voice processing, facsimile, text-to-speech (TTS), and automatic speech recognition (ASR). These boards share a common hardware and software architecture with other SCbus and CT Bus boards for maximum flexibility and scalability. You can add features and grow the system while protecting your investment in hardware and application code. Applications can be ported easily to lower or higher density platforms, with only minimum modifications.

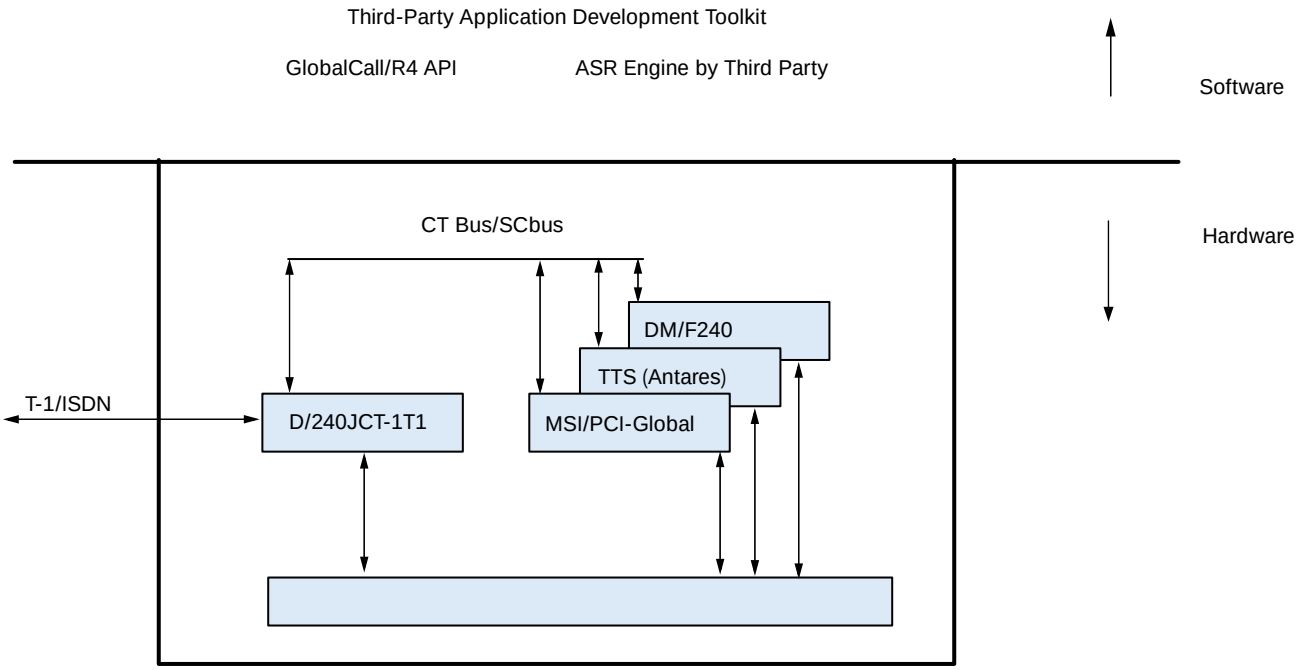
SingleSpan-JCT boards install in any PCI-based PC or server (PCI bus or mixed PCI/ISA bus) and compatible computers (Intel386™, Intel486™, or Pentium® processors or Sun UltraSPARC*). Each board occupies a single expansion slot and up to 16 boards can be configured in a system. The number of boards and channels supported varies depending on the application, the operating system, the amount of disk I/O required, the number of CT Bus loads per board, and the host computer's CPU(s), and power supply.

SingleSpan-JCT boards can operate in either terminate or drop-and-insert configurations. In a terminate configuration, the board handles the call processing of the digital audio and telephony signaling, facsimile, and the software-based speech recognition. If additional resources are required, such as TTS, these resources can be switched to the call via the CT Bus/SCbus. A SingleSpan-JCT board installed as a terminating device eliminates the need for a channel bank. The system operates as a standalone call processing node.

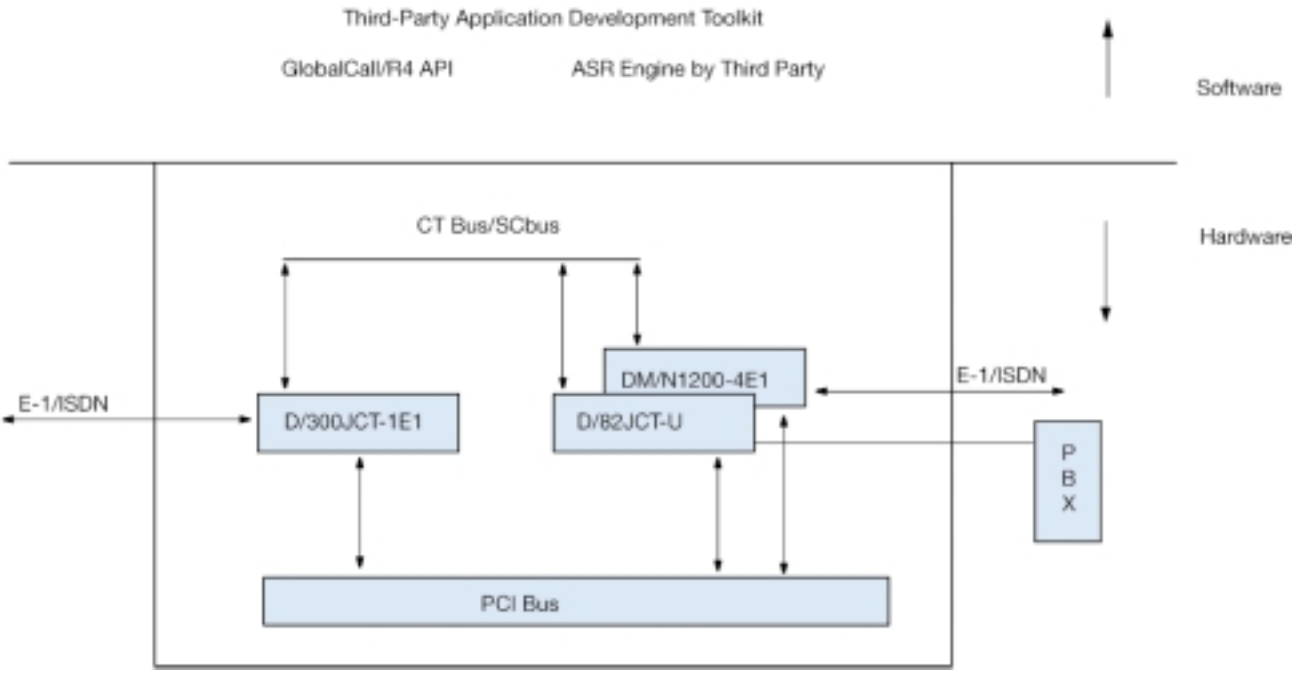
In a drop-and-insert configuration, use SingleSpan-JCT boards and a DTI board connected via the CT Bus/SCbus to pass T-1 or E-1 time slots through to each other. This configuration joins two separate T-1 or E-1 lines, or it can be placed in-line between a T-1 or E-1 line and a switch (a PBX, for example). Calls on individual channels can either terminate at a call processing resource on a SingleSpan-JCT series board, or "flow through" transparently to the DTI board.

Applications

- Messaging and enhanced services
- Voice portal
- Contact center and e-Business
- PC-PBX
- Switching and call completion
- Prepaid/debit card
- Gateway switch



Terminate Configuration



Drop-and-Insert Configuration

ISDN-PRI Support

The ISDN Primary Rate Interface (PRI) firmware is a standard feature of the SingleSpan-JCT Series. The PRI firmware is approved for use with many popular protocols in major market segments, based on both T-1 (1.544 Mb/s) and E-1 (2.048 Mb/s) physical interfaces.

Features and benefits of ISDN PRI include

- ISDN PRI connectivity to computer telephony (CT) systems
- Dialed Number Identification Service (DNIS) lets the application route incoming calls by automatically identifying the number the caller dialed
- Automatic Number Identification (ANI) lets the application identify the calling party
- ANI-on-Demand feature saves money by selectively requesting ANI information only when needed
- ISDN offers inherent benefits to call center applications with its fast call setup and fast retrieval of DNIS and ANI information on inbound calls
- Call-By-Call Service Selection lets an application select the most efficient bearer channel service on a call-by-call basis
- Subaddressing allows direct connection to individual extensions or devices sharing the same phone number, or as a proprietary messaging mechanism
- Powerful and universal software interface simplifies access for developers who are unfamiliar with ISDN, yet enables sophisticated control of features
- Multinational approvals with many popular protocols
- User-to-User Information lets an application send proprietary messages to remote systems during call establishment
- Facility, Notify, and optional Information Elements (IEs) let applications work with network-specific supplementary services
- Layer 2 access empowers developers to build customized Layer 3 protocol
- Ability to dynamically set protocol timers through host application programming interfaces (APIs)
- Programmable Startup Cause Value presentation to the network lets the user reject an incoming call with a preassigned cause value if the host has not yet done a waitcall on that channel
- Maskable Layer 2 Control lets the application toggle between bringing Layer 2 up and down as desired
- Support for SERVICE, SERVICE_ACK, and STATUS ENQUIRY messages

Software Support

Intel Dialogic SingleSpan-JCT boards are supported by the System Software and Software Development Kits (SDKs) for Windows NT*, Windows* 2000, and Linux*. These packages contain a set of tools for developing sophisticated, multimedia communications applications.

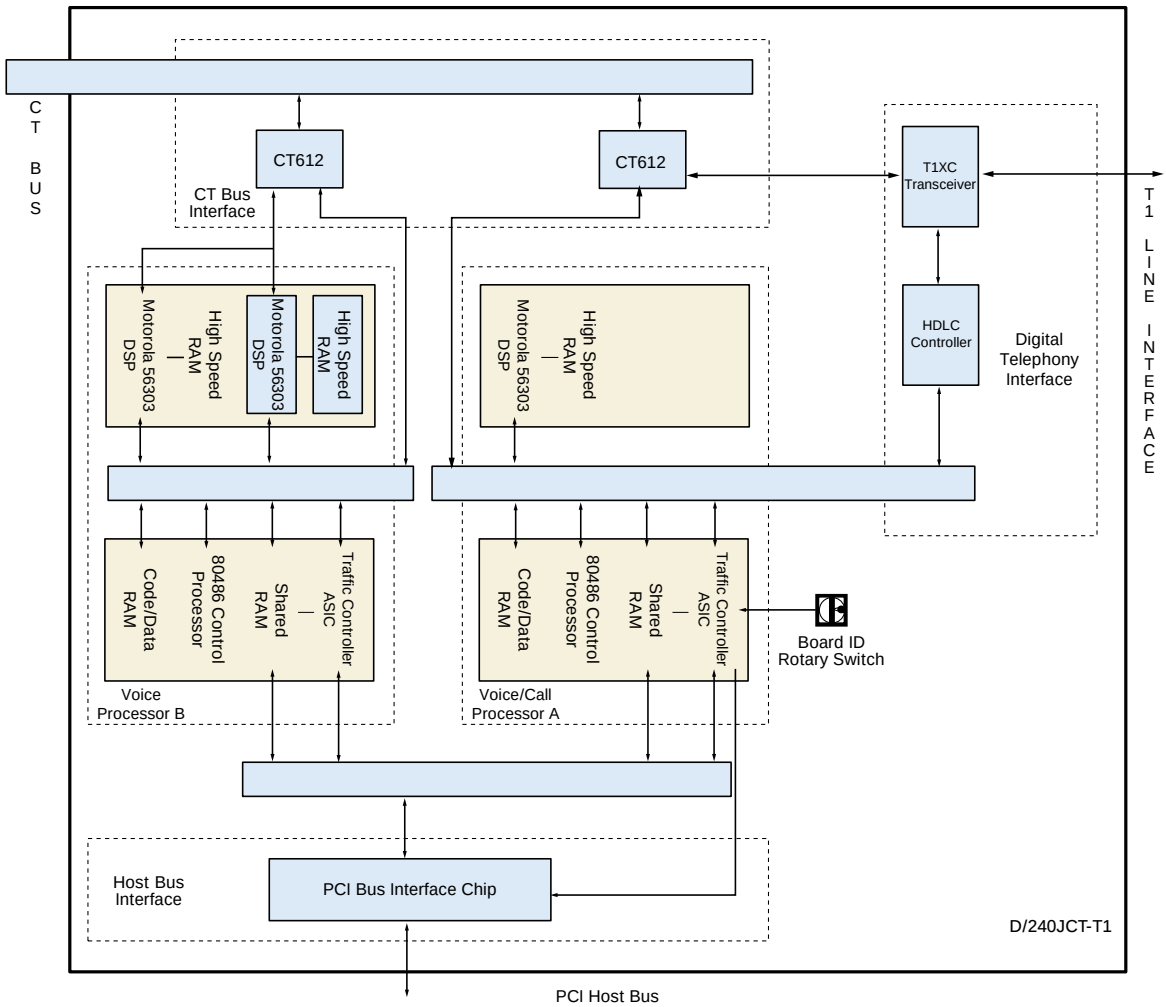
SingleSpan-JCT boards can use Global Call software as well as support Intel Dialogic CT Media server software which facilitates multiapplication development. These boards also support the Board Watch tool, the SNMP-compatible software for remote CT board management. Board Watch software simplifies the management of CT devices and lowers the total cost of operation. Centralized management capabilities provide a single point of configuration and inventory for all network devices. Fault management for high-availability systems includes diagnostics, detection, and recovery capabilities.

Global Call

The Single-Span JCT boards support Global Call software, a unified call control programming interface and protocol engine that makes it easier to provide worldwide application portability and can shorten development time by using the same application programming interface (API) for almost any network protocol.

Global Call software provides a common signaling interface for network-enabled applications, regardless of the signaling protocol needed to connect to the local telephone network. Global Call is the recommended API for unified call control for Spring Ware and DM3 architectures. The signaling interface provided by Global Call facilitates the exchange of call control messages between the telephone network and virtually any network-enabled application. Global Call lets developers create an application that can work with signaling systems worldwide, regardless of the network to which they are connected.

Global Call is ideal for high-density, network-enabled solutions for voice, data, and video, where the supported hardware and signaling technology can vary widely. Rather than requiring the application to handle the low-level details, Global Call software offers a consistent, high-level interface to the user, handling each country's unique protocol requirements in a way that is transparent to the application.



Functional Block Diagram

Functional Description

D/240JCT-T1

The Intel Dialogic D/240JCT-T1 board connects directly to a channel service unit (CSU), digital service unit (DSU), or to other network terminating equipment. The CSU chosen must support the D4 or ESF (within ISDN) superframe format. Most functions traditionally performed by a DSU (such as unipolar to bipolar format conversion, framing, etc.) are performed by the D/240JCT-T1 board. (The only exception is the ability to interpret certain bipolar violation patterns such as loop-back start and stop commands from the T-1 network.)

The board processes the digital on-hook/off-hook signaling information and digital voice signals from the telephone network. Digital T-1 signals enter the board via a T1XC line interface (see block diagram). The line interface contains a software-switchable clock that can be set to any of the following settings:

- loop (clocking is slaved to the external network)
- independent (clocking is derived from an onboard oscillator)
- expansion (clocking is slaved to another bus clock master board)

The incoming T-1 bit stream is applied to a CT612 chip, which acts as a traffic coordinator for each channel and as an interface to the CT Bus. This serial bit stream contains the digitized voice data and the signaling information for the incoming call.

Each of two CT612 functional modules on the D/240JCT-T1 board transmits several lower speed data streams over a single high-speed channel. The bus configuration is set when the firmware is downloaded at system initialization. These chips incorporate matrix switching capabilities. Under control of an onboard control processor, a CT612 functional module can connect a call being processed or an available

external resource to any of the CT Bus time slots. This lets the application route calls to any added resources such as fax, TTS, or ASR.

A DSP resource receives digital voice data via a CT612 module. The DSP processes the data based on Spring Ware firmware loaded in its high-speed RAM. Each DSP performs the following signal analysis and operations on this incoming data:

- applies automatic gain control (AGC) to compensate for variations in the level of the incoming audio signal
- applies an Adaptive Differential Pulse Code Modulation (ADPCM), Pulse Code Modulation (PCM), GSM, or G.726 algorithm to compress the digitized voice and save disk storage space
- detects the presence of tones — DTMF, MF, or an application-defined, single- or dual-frequency tone
- detects silence to determine whether the line is quiet and the caller is not responding

For outbound data, the DSP performs the following operations:

- expands stored, compressed audio data for play-back
- adjusts the volume and rate of speed of playback upon application or user request
- generates tones — DTMF, MF, or any application-defined, general-purpose tone

The dual processor combination also performs the following outbound dialing and call progress monitoring functions:

- transmits an off-hook signal to the telephone network
- dials out (makes an outbound call)
- monitors and reports call progress results
  - — line busy or congested
  - — operator intercept
  - — ring, no answer
  - — or if the call is answered, whether answered by a person, an answering machine, or a facsimile machine or modem

The board's line interface extracts or inserts telephony signaling information, which is processed by an onboard control processor. The DSPs only process the digitized voice data.

When recording speech, the DSP can use digitizing rates from 13 Kb/s to 64 Kb/s as selected by the application for the best speech quality and most efficient storage. The digitizing rate is selected on a channel-by-channel basis and can be changed each time a record or play function is initiated. The DSP-processed speech is transmitted by the control processor to the host PC for disk storage. When replaying a stored file, the processor retrieves the voice information from the host PC and passes it to the DSP, which converts the file into digitized voice. The DSP uses the CT Bus circuitry to send the digitized voice responses to the caller via the T1XC line interface.

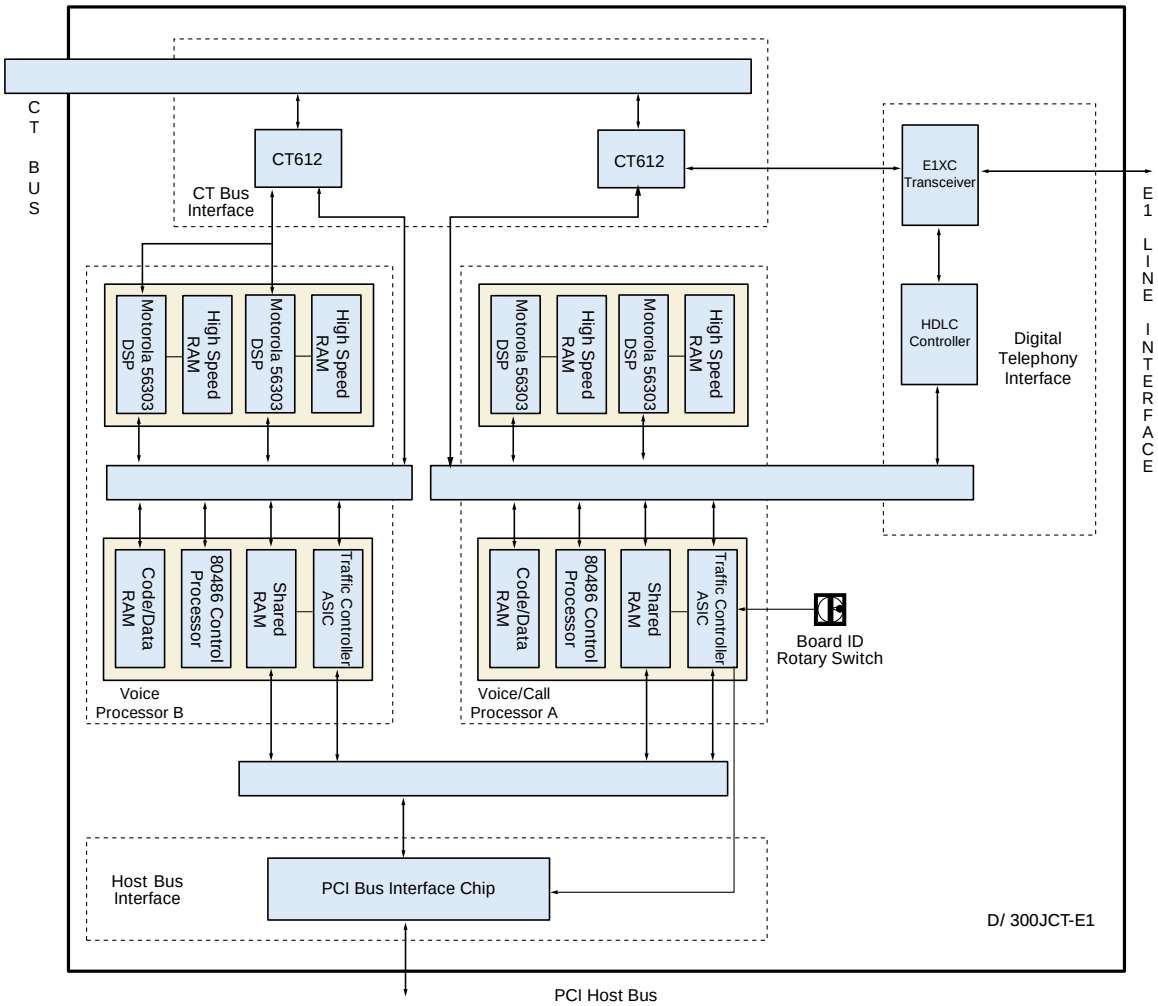
For CT Bus/SCbus configurations, the internal local buses operate at 2.048 Mb/s. A high-level data link controller (HDLC) formats ISDN data. The HDLC receives ISDN signaling data from the T1XC interface and CT612 ASIC and makes it available to the control processor. It also formats and sends outbound signaling data from the control processor to the network interface through the CT612 ASIC and T1XC transceiver chip.

The onboard control processor(s) controls all operations of the board via local buses and interprets and executes commands from the host PC. These processors

- handle real-time events
- manage data flow to the host PC to provide faster system response time
- reduce PC host processing demands
- process DTMF and telephony signaling before passing them to the application
- free the DSPs to perform signal processing

Communications between a processor and the host PC is via the shared RAM, which acts as an input/output buffer, increasing the efficiency of disk file transfers. This RAM interfaces to the host PC via the PCI bus. All operations are interrupt-driven to meet the demands of real-time systems. When the system is initialized, Spring Ware firmware is downloaded from the host PC to the onboard code/data RAM and DSP RAM to control all board operations. This firmware gives the board all of its intelligence and enables easy feature enhancement and upgrades.

The traffic controller ASIC is the Intel486 control processor interface that handles all peripheral devices (CT612, HDLC, DSPs, T1XC) and host PC functions (board locator technology, programmable interrupts, and shared RAM). The board locator technology circuit inside the traffic controller ASIC operates in conjunction with a rotary switch, eliminating the need to set confusing jumpers or DIP switches.



Functional Block Diagram

D/300JCT-E1

The Intel® Dialogic® D/300JCT-E1 board processes the digital on-hook/off-hook signaling information and digital voice signals from the telephone network. Digital E-1 signals enter the board via an E1XC line interface (see block diagram). The line interface supports CRC4 error detection (Cyclic Redundancy Check) and contains a software-switchable clock that can be set to any of the following settings:

- loop (clocking is slaved to the external network)
- independent (clocking is derived from an onboard oscillator)
- expansion (clocking is slaved to another bus clock master board)

Each of two CT612 functional modules on the D/300JCT-E1 board transmits several lower speed data streams over a single high-speed channel. The bus configuration is set when the firmware is downloaded at system initialization. These chips incorporate matrix switching capabilities. Under control of an onboard control processor, a CT612 functional module can connect a call being processed or an available external resource to any of the CT Bus time slots. This lets the application route calls to any added resources such as fax, TTS, or ASR.

A DSP resource receives digital voice data via a CT612 module. The DSP processes the data based on Spring Ware firmware loaded in its high-speed RAM. Each DSP performs the following signal analysis and operations on this incoming data:

- AGC to compensate for variations in the level of the incoming audio signal
- applies an ADPCM, PCM, GSM, or G.726 algorithm to compress the digitized voice and save disk storage space
- detects the presence of tones — DTMF, R2MF, or an application-defined, single- or dual-frequency tone
- detects silence to determine whether the line is quiet and the caller is not responding

For outbound data, the DSP performs the following operations:

- expands stored, compressed audio data for playback
- adjusts the volume and rate of speed of playback upon application or user request
- generates tones — DTMF, R2MF, or any application-defined, general-purpose tone

The dual processor combination also performs the following outbound dialing and call progress monitoring functions:

- transmits an off-hook signal to the telephone network
- dials out (makes an outbound call)
- monitors and reports call progress results
  - — line busy or congested
  - — operator intercept
  - — ring, no answer
  - — or if the call is answered, whether answered by a person, an answering machine, or a facsimile machine or modem

The board's line interface extracts or inserts telephony signaling information, which is processed by an onboard control processor. The DSPs only process the digitized voice data.

When recording speech, the DSP can use digitizing rates from 13 Kb/s to 64 Kb/s as selected by the application for the best speech quality and most efficient storage. The digitizing rate is selected on a channel-by-channel basis and can be changed each time a record or play function is initiated. The DSP-processed speech is transmitted by the control processor to the host PC for disk storage. When replaying a stored file, the processor retrieves the voice information from the host PC and passes it to the DSP, which converts the file into digitized voice. The DSP uses the CT Bus circuitry to send the digitized voice responses to the caller via the E1XC line interface.

For CT Bus/SCbus configurations, the internal local buses operate at 2.048 Mb/s. An HDLC formats ISDN data. The HDLC receives ISDN signaling data from the E1XC interface and CT612 ASIC and makes it available to the control processor. It also formats and sends outbound signaling data from the control processor to the network interface through the CT612 ASIC and E1XC transceiver chip.

The onboard control processor(s) controls all operations of the board via local buses and interprets and executes commands from the host PC. These processors

- handle real-time events
- manage data flow to the host PC to provide faster system response time
- reduce PC host processing demands
- process DTMF and telephony signaling before passing them to the application
- free the DSPs to perform signal processing

Communications between a processor and the host PC is via the shared RAM, which acts as an input/output buffer, increasing the efficiency of disk file transfers. This RAM interfaces to the host PC via the PCI bus. All operations are interrupt-driven to meet the demands of real-time systems. When the system is initialized, Spring Ware firmware is downloaded from the host PC to the onboard code/data RAM and DSP RAM to control all board operations. This firmware gives the board all of its intelligence and enables easy feature enhancement and upgrades.

The traffic controller ASIC is the Intel486 control processor interface that handles all peripheral devices (CT612, HDLC, DSPs, E1XC) and host PC functions (board locator technology, programmable interrupts, and shared RAM). The board locator technology circuit inside the traffic controller ASIC operates in conjunction with a rotary switch, eliminating the need to set confusing jumpers or DIP switches.

Technical Specifications** for D/240JCT-T1

	Number of ports	24
	Max. boards/system	16. Number may be limited by application, system performance, and the number of CT Bus loads per board.
	CT Bus loads per board	1.5
	Maximum CT Bus loads per system	20 (See CT Bus specification for further details.)
	Digital network interface	Onboard DSX-1 interface
	Resource sharing bus	H.100 CT Bus
	Control processors	Two Intel486™ GX processors @ 32.7 MHz, 0 wait state
	Digital signal processors	Three Motorola* DSP56303 @ 100 MHz, each with 256 K word private, 2 wait state SRAM
Host Interface		
	Bus compatibility	PCI. Complies with PCISIG* Bus Specification, Rev. 2.2.
	Bus speed	33 MHz maximum
	Bus mode	32- to 16-bit conversion in target mode
	Shared memory	2 × 64 KB page
	I/O ports	None
	Support	3.3 V or 5 V signaling environment (universal connectivity)
Telephone Interface		
	Clock rate	1.544 Mb/s ±32 ppm
	Level	3.0 V (nominal)
	Pulse width	323.85 ns (nominal)
	Line impedance	100 Ohm ±10%
	Other electrical characteristics	Complies with AT&T* TR62411 and ANSI T1.403-1989
	Framing	SF (D3/D4) ESF for ISDN
	Line coding	AMI AMI with B7 stuffing B8ZS
	Clock and data recovery	Complies with AT&T TR62411 and Bellcore* TA-TSY-000170
	Jitter tolerance	Complies with AT&T TR62411 and ANSI T1.403-1989
	Connectors	RJ-48C
	Telephony bus connector	H.100-style 68-pin fine pitch card edge connector
	Loopback	Supports switch-selectable local analog loopback and software selectable local digital loopback
Power Requirements		
	+5 VDC	2.0 A typical; 2.2 A maximum
	+12 VDC	6 mA typical; 6.6 mA maximum
	–12 VDC	Not required
	Operating temperature	0°C to +50°C
	Storage temperature	–20°C to +70°C
	Humidity	8% to 80% noncondensing
	Form factor	PCI long card
		12.3 in. long (30.75 cm) (without edge retainer) or 13.3 in. long (33.25 cm) (with edge retainer) 0.79 in. wide (1.975 cm) (total envelope) 3.87 in. high (9.675 cm) (excluding edge connector)

Technical Specifications** for D/240JCT-T1 (cont.)

Safety and EMI Certification

United States	FCC part 68 ID#: EBZUSA-20078-XD-N UL: 1950 (E96804)
Canada	IC: 885 5959 A CSA 950 (E96804)
Estimated MTBF	150,000 hours per Bellcore Method I
Warranty	Intel® Telecom Products Warranty Information at http://www.intel.com/network/csp/products/3144web.htm

Technical Specifications** for D/300JCT-E1

Number of ports	30
Max. boards/system	16. Number may be limited by application, system performance, and the number of CT Bus loads per board.
CT Bus loads per board	1.5
Maximum CT Bus loads per system	20 (See CT Bus specification for further details.)
Digital network interface	Onboard E-1 interface
Resource sharing bus	H.100 CT Bus
Control processors	Two Intel486™ GX processors @ 32.7 MHz, 0 wait state
Digital signal processors	Three Motorola* DSP56303 @ 100 MHz, each with 256 K word private, 2 wait state SRAM

Host Interface

Bus compatibility	PCI. Complies with PCISIG* Bus Specification, Rev. 2.2.
Bus speed	33 MHz maximum
Bus mode	32- to 16-bit conversion in target mode
Shared memory	2 × 64 KB page
I/O ports	None
Support	3.3 V or 5 V signaling environment (universal connectivity)

Telephone Interface

Network clock rate	2.048 Mb/s ±50 ppm
Internal clock rate	2.048 Mb/s ±32 ppm
Level	2.37 V (nominal) for 75 Ohm lines 3.0 V (nominal) for 120 Ohm lines
Pulse width	244 ns (nominal)
Line impedance	75 Ohm, unbalanced 120 Ohm, balanced
Other electrical characteristics	Complies with CCITT Rec. G. 703
Framing	CCITT G. 704-1988 with CRC4
Line coding	HDB3
Clock and data recovery	Complies with CCITT Rec. G.823-1988
Jitter tolerance	Complies with CCITT Rec. G.823, G.737, G.739, G.742-1988
Connectors	BNC for 75 Ohm lines RJ-48C for 120 Ohm lines
Telephony bus connector	H.100-style 68-pin fine pitch card edge connector
Loopback	Supports switch-selectable local analog loopback and software selectable local digital loopback

Technical Specifications** for D/300JCT-E1 (cont.)

Power Requirements

+5 VDC	2.0 A typical; 2.2 A maximum
+12 VDC	6 mA typical; 6.6 mA maximum
–12 VDC	Not required
Operating temperature	0°C to +50°C
Storage temperature	–20°C to +70°C
Humidity	8% to 80% noncondensing
Form factor	PCI long card 12.3 in. long (30.75 cm) (without edge retainer) or 13.3 in. long (33.25 cm) (with edge retainer) 0.79 in. wide (1.975 cm) (total envelope) 3.87 in. high (9.675 cm) (excluding edge connector)

Safety and EMI Certification

United States	FCC part 68 ID#: EBZUSA-20078-XD-N UL: 1950 (E96804)
Canada	IC: 885 5959 A UL: CSA 950 (E96804)
Estimated MTBF	150,000 hours per Bellcore Method I
Warranty	Intel® Telecom Products Warranty Information at http://www.intel.com/network/csp/products/3144web.htm

Spring Ware Firmware Technical Specifications**

Facsimile

Fax compatibility	ITU-T G3 compliant (T.4, T.30) ETSI NET/30 compliant
Data rate	14,400 b/s (v.17) send 9600 b/s receive
Variable speed selection	Automatic step-down to 12,000 b/s, 9600 b/s, 7200 b/s, 4800 b/s, and lower
Transmit data modes	Modified Huffman (MH) Modified Read (MR)
Receive data modes	MH MR
File data formats	Tagged Image File Format (TIFF/F) for transmit/receive MH and MR
ASCII-to-fax conversion	Host-PC-based conversion Direct transmission of text files All Windows* fonts supported Page headers generated automatically
Error correction	Detection, reporting, and correction of faulty scan lines
Image widths	8.5 in. (21.25 cm) 10 in. (25 cm) 11.9 in. (29.75 cm)
Image scaling	Automatic horizontal and vertical scaling between page sizes
Polling modes	Normal Turnaround
Image resolution	Normal (203 pels/in. × 98 lines/in.) Fine (203 pels/in. × 196 lines/in.)
Fill minimization	Automatic fill bit insertion and stripping

Spring Ware Firmware Technical Specifications** (cont.)

Audio Signal		
	Receive range	(T-1) –40 dBm0 to +2.5 dBm0 nominal, configurable by parameter† (E-1) –43 dBm0 to +2.5 dBm0 nominal, configurable by parameter†
	Automatic gain control	Application can enable/disable. Above –18 dBm0 (T-1) or –21 dBm0 (E-1) results in full-scale recording, configurable by parameter.†
	Silence detection	–38 dBm0 nominal, software adjustable†
	Transmit level (weighted average)	(T-1) –9 dBm0 nominal, configurable by parameter† (E-1) –12.5 dBm0 nominal, configurable by parameter†
	Transmit volume control	40 dB adjustment range, with application-definable increments and legal limit cap
Frequency Response		
	24 Kb/s	300 Hz to 2600 Hz ±3 dB
	32 Kb/s	300 Hz to 3400 Hz ±3 dB
	48 Kb/s	300 Hz to 2600 Hz ±3 dB
	64 Kb/s	300 Hz to 3400 Hz ±3 dB
Audio Digitizing		
	13 Kb/s	GSM @ 8 kHz sampling
	24 Kb/s	OKI ADPCM @ 6 kHz sampling
	32 Kb/s	OKI ADPCM @ 8 kHz sampling
	32 Kb/s	G.726 @ 8 kHz sampling
	48 Kb/s	A-law PCM @ 6 kHz sampling
	64 Kb/s	A-law PCM @ 8 kHz sampling
	48 Kb/s	µ-law PCM @ 6 kHz sampling
	64 Kb/s	µ-law PCM @ 8 kHz sampling
	Digitization selection	Selectable by application on function call-by-call basis
	Playback speed control	Pitch controlled Available for 24 Kb/s and 32 Kb/s data rates Adjustment range: ±50% Adjustable through application or programmable DTMF control
DTMF Tone Detection		
	DTMF digits	0 to 9, *, #, A, B, C, D per CCITT Q.23
	Dynamic range	(T-1) –36 dBm0 to –3 dBm0 per tone, configurable by parameter† (E-1) –39 dBm0 to 0 dBm0 per tone, configurable by parameter†
	Minimum tone duration	40 ms, can be increased with software configuration
	Interdigit timing	Detects like digits with a 40 ms interdigit delay. Detects different digits with a 0 ms interdigit delay.
	Acceptable twist and frequency variation	(T-1) Meets Bellcore LSSGR Sec 6 and EIA 464 requirements (E-1) Meets appropriate CCITT specifications†
	Noise tolerance	Meets Bellcore LSSGR Sec 6 and EIA 464 requirements for Gaussian, impulse, and power line noise tolerance
	Cut-through	(T-1) Local echo cancellation permits 100% detection with a >4.5 dB return loss line (E-1) Digital trunks use separate transmit and receive paths to network. Performance dependent on far-end handset's match to local analog loop.
	Talk off	Detects less than 20 digits while monitoring Bellcore TR-TSY-000763 standard speech tapes. (LSSGR requirements specify detecting no more than 470 total digits.) Detects 0 digits while monitoring MITEL speech tape #CM 7291.

Spring Ware Firmware Technical Specifications** (cont.)

Global Tone Detection		
	Tone type	Programmable for single or dual
	Max. number of tones	Application-dependent
	Frequency range	Programmable within 300 Hz to 3500 Hz
	Max. frequency deviation	Programmable in 5 Hz increments
	Frequency resolution	±5 Hz. Separation of dual frequency tones is limited to 62.5 Hz at a signal-to-noise ratio of 20 dB.
	Timing	Programmable cadence qualifier, in 10 ms increments
	Dynamic range	(T-1) Programmable, default set at –36 dBm0 to –0 dBm0 (single tone), –3 dBm0 (dual tone) (E-1) Programmable, default set at –39 dBm0 to +0 dBm0 per tone
Global Tone Generation		
	Tone type	Generate single or dual tones
	Frequency range	Programmable within 200 Hz to 4000 Hz
	Frequency resolution	1 Hz
	Duration	10 ms increments
	Amplitude	(T-1) –43 dBm0 to –3 dBm0 per tone nominal, programmable (E-1) –40 dBm0 to +0 dBm0 per tone nominal, programmable
MF Signaling (T-1)	**R1**	
	MF digits	0 to 9, KP, ST, ST1, ST2, ST3 per Bellcore LSSGR Sec 6, TR-NWT-000506 and CCITT Q.321
	Transmit level	Complies with Bellcore LSSGR Sec 6, TR-NWT-000506
	Signaling mechanism	Complies with Bellcore LSSGR Sec 6, TR-NWT-000506
	Dynamic range for detection	–25 dBm0 to –3 dBm0 per tone
	Acceptable twist	6 dB
	Acceptable freq. variation	Less than ±1 Hz
MF Signaling (E-1)	**R2**	
	MF digits	All 15 forward and backward signal tones per CCITT Q.441
	Transmit level	–8 dBm0 per tone, nominal, per CCITT Q.454; programmable
	Signaling mechanism	Supports the R2 compelled signaling cycle and non-compelled pulse requirements per CCITT Q.457 and Q.442
	Dynamic range for detection	–35 dBm0 to –5 dBm0 per tone
	Acceptable twist	6 dB
	Acceptable freq. variation	Less than ±1 Hz

Spring Ware Firmware Technical Specifications** (cont.)

Call Progress Analysis

Busy tone detection	Default setting designed to detect 74 out of 76 unique busy/congestion tones used in 97 countries as specified by CCITT Rec. E., Suppl. #2. Default uses both frequency and cadence detection. Application can select frequency only for faster detection in specific environments.
Ring back detection	Default setting designed to detect 83 out of 87 unique ring back tones used in 96 countries as specified by CCITT Rec. E., Suppl. #2. Uses both frequency and cadence detection.
Positive voice detection accuracy	>99% based on tests on a database of real world calls in North America. Performance in other markets may vary.
Positive voice detection speed	Detects voice in as little as 1/10th of a second
Positive answering machine detection accuracy	85% based on tests on a database of real world calls in North America. Performance in other markets may vary.
Fax/modem detection	Preprogrammed
Intercept detection	Detects entire sequence of the North American tri-tone. Other SIT tones can be programmed.
Dial tone detection before dialing	Application enable/disable Supports up to three different user-definable dial tones Programmable dial tone drop out debouncing

Tone Dialing

DTMF digits	0 to 9, *, #, A, B, C, D per Bellcore LSSGR Sec 6, TR-NWT-000506
Frequency variation	Less than ±1 Hz
Rate	10 digits/s, configurable by parameter†
Level	–7.5 dBm0 per tone, nominal, configurable by parameter†

Pulse Dialing

10 digits	0 to 9
Pulsing rate	10 pulses/s, nominal, configurable by parameter†
Break ratio	60% nominal, configurable by parameter†

Analog Display Services Interface (ADSI)

FSK generation per Bellcore TR-NWT-000030
CAS tone generation and DTMF detection per Bellcore TR-NWT-001273

** All specifications are subject to change without notice.
† Configurable to meet country-specific PTT requirements. Actual specification may vary from country to country for approved products.

Hardware System Requirements

- Intel386™, Intel486™, or Pentium® microprocessor PCI bus or mixed PCI/ISA bus computer
- Operating system hardware requirements vary according to the number of channels being used
- System must comply with PCISIG Bus Specification Rev. 2.1 or later

Additional Components (with Item Market Names)

- Multidrop CT Bus cables (CBLCTB68C3DROP, CBLCTB68C4DROP, CBLCTB68C8DROP, CBLCTB68C12DROP, CBLCTB68C16DROP)
- CT Bus/SCbus adapter (CTBUSTOSCBUSADP)
- SCbus terminator kits (1SCBUS1TERMKIT, 2SCBUS1TERMKIT, 3SCBUS1TERMKIT)

To learn more, visit our site on the World Wide Web at **www.intel.com**

1515 Route Ten
Parsippany, NJ 07054
Phone: 1-973-993-3000
Fax: 1-973-993-3093

Printed in the USA Printed on recycled paper. 11/02 00-6038-006